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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/087,432	03/01/2002	Sung-Fei Wang	U 013887-9	3547

7590 07/20/2005

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EXAMINER	
MITCHELL, JAMES M	
ART UNIT	PAPER NUMBER
2813	

DATE MAILED: 07/20/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/087,432	WANG ET AL.	
	Examiner	Art Unit	
	James M. Mitchell	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 June 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *5-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *5-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This office action is in response to the advisory action filed June 24, 2005.

Allowable Subject Matter

The indicated allowability of claims 5-10 are withdrawn in view of the newly discovered reference(s) to Huang et al. (U.S. 6,650,006), Nakanishi (U.S. 6,072,243) and Hiraoka (U.S. 6,740,970). Rejections based on the newly cited reference(s) follow. The finality of the last action is withdrawn.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 5 and 6 are rejected under 35 U.S.C. 102(e) as being clearly anticipated by Huang et al. (U.S. 6,650,006 in Fig. 4 &5).

Claim 5 rejected under 35 U.S.C. 102(e) as being anticipated by Nakanishi (U.S. 6,072,243).

Nakanishi (Fig. 1a, b) discloses: a substrate having a top surface; a stacked semiconductor chip package comprising: a first chip (8) on the top surface of the substrate and electrically connected (50) to the leads that provide support and therefore a substrate; a second chip (7) disposed above the first chip and electrically connected to the substrate and having two opposed longitudinal sides defining a first length; and a plate (11) between the first chip and the second chip, physically connected to the first chip and the second chip directly by adhesive (60), and having two opposed longitudinal sides corresponding to the two longitudinal sides of the second chip, the plate defining a second length, the second length being larger than the first length to expose the opposed longitudinal sides of the plate and to expose the adhesive between the plate and the second chip (Fig. 1b), wherein the portion of the plate under the second chip is wrapped in the adhesive (i.e. encapsulant covers plate and chips), and the adhesive is made visible and therefore exposed at the corner formed by the plate and second chip along the longitudinal side of the plate.

Claims 7 and 8 are rejected under 35 U.S.C. 102(e) as being anticipated by Hiraoka (U.S. 6,740,970).

Hiraoka (Fig. 1, 2) discloses:

(cl. 7) a stacked semiconductor chip package comprising: a substrate (12) having a top surface; a first chip (18) on the top surface of the substrate and electrically connected (32) to the substrate; a second chip (22) disposed above the first chip and electrically connected (34) to the substrate and having two opposed longitudinal sides (i.e.

horizontal portion) defining a first length; and a plate (431) between the first chip and the second chip connected to the first chip and the second chip (i.e. in physical contact), and having two opposed longitudinal sides (i.e. horizontal portion) corresponding to the two longitudinal sides of the second chip, the plate defining a second length, the second length being larger than the first length (Fig. 2) to expose the opposed longitudinal sides of the plate and to expose adhesive layer (36) formed between the plate and the second chip, wherein the portion of the plate under the second chip is wrapped in the adhesive layer (i.e. encapsulant wraps plate and chip), and the adhesive layer is visible and therefore exposed at the corner formed by the plate and second chip along the longitudinal side of the plate, wherein corresponding to the two longitudinal sides of the second chip, the second chip further has two opposed transverse sides defining a first width (i.e. vertical portion), the plate further has two opposed transverse sides defining a second width smaller than the first width (Fig. 2);

(cl. 8) and the first chip has two opposed transverse sides defining a third width and the second with is smaller than the second width (i.e. plate is thinner the first and second chips; Fig. 2).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 6-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Huang (U.S. 6,650,006) in combination with Hiraoka (U.S. 6,740,970).

Huang (Fig. 4-7) discloses:

(cl. 6, 7) a stacked semiconductor chip package comprising: a substrate (not labeled in Fig. 5) having a top surface; a first chip (61) on the top surface of the substrate and electrically connected to the substrate; a second chip (64) disposed above the first chip and electrically connected to the substrate and having two opposed longitudinal sides (i.e. horizontal portion) defining a first length; and a plate (431) between the first chip and the second chip connected to the first chip and the second chip (i.e. in physical contact), and having two opposed longitudinal sides (i.e. horizontal portion) corresponding to the two longitudinal sides of the second chip, the plate defining a second length, the second length being larger than the first length (Fig. 4) to expose the opposed longitudinal sides of the plate and to expose adhesive layer (46) formed between the plate and the second chip, wherein the portion of the plate under the second chip is wrapped in the adhesive layer (i.e. encapsulant wraps plate and chip), and the adhesive layer is visible and therefore exposed at the corner formed by the plate and second chip along the longitudinal side of the plate, wherein corresponding to the two longitudinal sides of the second chip, the second chip further has two opposed transverse sides defining a first width (i.e. vertical portion), the plate further has two opposed transverse sides defining a second width;

(cl. 8, 10) wherein the first chip further has two opposed transverse sides defining a third width (i.e. horizontal portion).

Huang doe not disclose the second width being smaller than the first width [*i.e. second chip above first*] / or the width of the first chip.

Hiraoka (Fig.2) utilizes a plate (20) with a second width being smaller than the first width (of item 22) or the width of the first chip width [*i.e. first chip below second chip*] / or the width of the first chip.

It would have been obvious to one of ordinary skill in the art to form the plate of Huang with a second width smaller than the first width or the width of the first chip in order to permit cooling of the device as taught by Hiraoka (Col. 7, Lines 17-19).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The prior art in Sinai (JP404056262) discloses a stack semiconductor chip package wherein a portion of a plate and chip is wrapped in an adhesive.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to James M. Mitchell whose telephone number is (571) 272-1931. The examiner can normally be reached on M-F 8:00-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead Jr. can be reached on (571) 272-1702. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jmm
July 5, 2005

CARL WHITEHEAD, JR.
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